Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A line ~~Line~~ driver ~~arrangement (1)~~ for driving signals ~~(Vi, Vo)~~ via at least one subscriber line ~~(4)~~, ~~having~~ comprising:

an input ~~(2)~~ for injecting an input signal ~~(Vi)~~ and ~~having~~ an output ~~(3)~~ at which a signal ~~(Vo)~~ which is to be driven via the subscriber line ~~(4) can be~~ is tapped off,

a digital amplifier ~~(6)~~ which produces a ~~pulse-width-modulated~~ digital signal ~~(Vd, id)~~ on the output side from one of the input signal ~~(Vi)~~ or ~~from~~ a signal ~~(Vs)~~ derived from ~~it~~ the input signal,

an analog amplifier ~~(5)~~, which produces an analog signal ~~(Ve', ia)~~ on the output side from one of the input signal ~~(Vi)~~ or ~~from~~ a signal derived from ~~it~~ the input signal,

wherein ~~with~~ the outputs of the amplifiers ~~(5, 6) being~~ are coupled such that the signal ~~(Vo)~~ to be driven results from superimposition of the analog signal ~~(Ve', ia)~~ and the digital signal ~~(Vd, id)~~, and

wherein ~~with~~ the gain of the analog amplifier ~~(5) being~~ is matched to the gain of the digital amplifier ~~(6)~~ such that at least one of the scatter ~~and/or~~ or overshoot on the digital signal ~~(Vd, id) are~~ is at least reduced after the superimposition.

2. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 1, and further comprising ~~characterized in that~~ a feedback path ~~(16) is provided,~~

via which the signal ~~(Vo, io)~~ which results from the superimposition of the analog and digital signals ~~(Ve', ia; Vd, id) can be~~ is fed back with negative feedback to the input of the analog amplifier ~~(5)~~.

3. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 2, wherein the analog amplifier ~~(5)~~ is arranged in an analog path ~~(10)~~, and the digital amplifier ~~(6)~~ is arranged in a digital path ~~(11)~~, with the two paths ~~(10, 11)~~ being arranged in parallel with one another.

4. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 3, ~~characterized in that~~ and further comprising a filter ~~(12), in particular a low-pass filter, is provided, follows~~ following the digital amplifier ~~(6)~~ in the digital path ~~(11)~~ and ~~carries~~ carrying out frequency smoothing as well as filtering of the digital signal ~~(Vd)~~.

5. (currently amended) The line ~~Line~~ driver ~~arrangement according to one~~ of Claim ~~Claims~~ 3 ~~or 4~~, ~~characterized in that~~ and further comprising a matching circuit ~~(14) is provided, is~~ connected upstream of the analog amplifier ~~(5)~~ in the analog path ~~(10)~~ and ~~carries~~ carrying out at least one of phase matching ~~and/or~~ or amplitude matching of the input signal ~~(Vi)~~ to the output signal ~~(Vo)~~.

6. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, wherein the analog amplifier ~~(5)~~ is followed by a resistance network ~~(40)~~, at whose output an analog current ~~(ia) can be~~ is tapped off, and ~~in that~~ wherein a potential ~~(Vs)~~ which is tapped off from the resistance network ~~(40) can be~~ is injected into the digital amplifier ~~(6), which uses this~~ to

produce on the output side a digital current ~~(id)~~ which is superimposed on the analog current ~~(ia)~~.

7. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 6, ~~characterized in that~~ wherein the resistance network ~~(40)~~ has at least one measurement resistance ~~(44)~~ via which the analog current ~~(ia)~~ is passed, and has a voltage divider ~~(45)~~ across which the potential ~~(Vs)~~ which is injected into the digital amplifier ~~(6)~~ ~~can be~~ is tapped off.

8. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 7, ~~characterized in that~~ wherein the resistance value of the measurement resistance ~~(44)~~ is very much less than the resistance values of the voltage divider resistances ~~(45)~~.

9. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, and further comprising at least one transformer ~~(13, 15) is~~ provided at the output ~~(3)~~ of the line driver ~~(1)~~.

10. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 2, and further comprising a load which is in the form of a transformer ~~(13) is~~ provided at the output ~~(3)~~ of the ~~power~~ line driver ~~arrangement (1)~~.

11. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of Claims 9 or 10, characterized in that~~ of Claim 9, wherein the transformer ~~(13)~~ is designed such that its bandwidth matches the bandwidth of the signal ~~(Vi, Vo)~~ to be driven.

12. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of Claims 9 to 11, characterized in that~~ of Claim 9, wherein at least one transformer ~~(13)~~ has a very high transformation ratio in the region of at least 1:4~~, in particular in the region of more than 1:6,~~ between the primary and the secondary sides.

13. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 11 and further comprising a further transformer ~~(15) is provided, is~~ arranged in the analog path ~~(10), and follows~~ following the analog amplifier ~~(5)~~.

14. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 13, ~~characterized in that~~ wherein the further transformer ~~(15)~~ has a lower transformation ratio than the first transformer ~~(13), in particular a transformation ratio of about 1:1~~.

15. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 14, and further comprising a divider ~~(18) is~~ provided in the feedback path ~~(16), and has~~ having a feedback factor ~~(f)~~ by which the fed-back signal is divided.

16. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 15, ~~characterized in that~~ wherein the feedback factor (f) corresponds to the transformation ratio of the transformer which follows the digital amplifier ~~(6)~~.

17. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 10, further comprising ~~the power driver arrangement (1) has~~ a further feedback device ~~(28)~~ which feeds back the

output signal ~~(Vo)~~ with positive feedback to the input ~~(2)~~, with the elements of the control loop which results from this being designed such that the impedance of the ~~power~~ line driver ~~arrangement (1)~~ is variable.

18. (currently amended) The line ~~Line~~ driver ~~arrangement according to~~ of Claim 17, ~~characterized in that [lacuna] for~~ wherein the variable impedance has a synthesis factor (m) which is proportional to the ratio of the load ~~(26)~~ to an output resistance ~~(25)~~.

19. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, and further comprising a control device ~~(8) is provided for~~ controlling the amplifiers ~~(5, 6)~~.

20. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, wherein the analog amplifier ~~(5)~~ is in the form of an inverting amplifier.

21. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 19, wherein the digital amplifier ~~(6)~~ has a comparator ~~(30, 50) which is~~ coupled to the input of the digital amplifier ~~(6) and is~~ followed, as the output stage ~~(31, 32; 51, 52)~~, by a power inverter.

22. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, wherein the digital amplifier ~~(6)~~ has a PWM characteristic, such that its digital output signals ~~(Vd, id)~~ are pulse-width modulated.

23. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, wherein the line driver ~~arrangement (1)~~ is in the form of an ADSL driver circuit.

24. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 22, wherein circuit means are provided, by means of which the switching frequency is matched to the amplitude of the output signal.

25. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, wherein the signals ~~(Vi, Vo)~~ to be driven are speech signals ~~and/or~~ or data signals.

26. (currently amended) The line ~~Line~~ driver ~~arrangement according to one of the preceding claims, characterized in that~~ of Claim 3, wherein the line driver ~~arrangement (1)~~ is completely differential.

27. (new) The line driver of Claim 9, wherein at least one transformer has a very high transformation ratio in the region of more than 1:6, between the primary and the secondary sides.

28. (new) The line driver of Claim 13, wherein the further transformer has a transformation ratio of about 1:1.

29. (new) A line driver for driving signals via a subscriber line, comprising:

an input for injecting an input signal;

an output at which a signal which is to be driven via the subscriber line is tapped off;

a digital path between the input and output including a digital amplifier which produces a pulse-width-modulated (PWM) signal on an output side of the digital path from a signal derived from the input signal;

an analog path between the input and output including an analog amplifier which produces an analog signal on an output side of the analog path from a signal derived from the input signal;

wherein the digital path and analog paths are arranged in parallel with one another and are coupled at their output sides such that the signal to be driven results from superimposition of the analog signal and the PWM signal; and

wherein the gain of the analog amplifier is matched to the gain of the digital amplifier such that at least one of the scatter or overshoot on the PWM signal is at least reduced after the superimposition.

30. (new) The apparatus of claim 29 and further comprising a feedback path via which the signal which results from the superimposition of the analog and PWM signals is fed back with negative feedback to an input of the analog path.